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Filing Date	February 26, 2004		
First Named Inventor	Guenter Stenz		
Art Unit	2825		
Examiner Name	Vuthe Siek		
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Examiner Initials *	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T2		
<b>/</b> />		Hiroshi Murata et al.; "VLSI Module Placement Based on Rectangle-Packing by the Sequence-Pair"; IEEE Transactions on computer-Aided Design of Integrated Circuits and Systems; Vol. 15, No. 2; December 1996; pp. 1518-1524.			
K		S. Kirkpatrick et al.; "Optimization by Simulated Annealing"; Science; Volume 220, Number 4598; 13 May 1983; pp. 671-680.			
15.		Dieter Jungnickel; Graphs, Networks and Algorithms; "Algorithms and Computation in Mathematics"; Chapter 13 - Weighted Matchings; Volume 5; Copyright 1999; published by Springer-Verlag Berlin Heidelberg New York; pp. 389-401.			
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